IN THE SPECIFICATION:

Please replace the Title of the Invention with the following new title:

DATA PROCESSOR FOR REDUCING SET-ASSOCIATIVE CACHE ENERGY VIA SELECTIVE WAY-PREDICTION

Please amend page 7, 2nd paragraph as follows:

The associative operation is, for example, an operation in which predetermined ~~address information contained in~~ access addresses are ~~information is~~ compared with tag information [[for]] contained in respective ways of the indexed cache line to generate an association result signal ~~indicative of~~ which indicates an association hit or association miss on a way basis.

Please amend page 20, 1st full paragraph as follows:

The history information storage part 13 holds way selection history information (matching ways selected via associative operation) on a cache line basis which may be stored, for example, in a Hit-Way History Table, so that the history information will be selected by the index address signal in response to the indexing operation of the cache line. Since it is two-way in this example, the history information [[is]] contains just one bit to generate the way prediction signal 22 from the history information selected by the index address. The way prediction signal 22 is a signal, which represents the least recently selected way for the corresponding cache line.

Please amend page 25, 1st full paragraph as follows:

Fig. 3 illustrates the details of the cache control part 12. The cache control part 12 is roughly divided into the way determination generating part 30 and a state transition controlling part (state machine) 31 as the other control part. In the way determination generating part 30, latch circuits 32A, 32B for latching the association result signals 19A, 19 are representatively shown in the drawing, indicating input of the access completion signal 25 and output of the way determining signal 23 from and to the CPU. The latch circuits 32A, 32B perform the latch operation in a cycle two cycles later than a cycle in which the access completion signal 25 is negated from a high level to a low level. In other words,

since the access complete signal 25 is negated from the access starting point, the latch operation is performed at such timing as to take in an address for the subsequent access in a cycle following the cycle in which the miss occurred. This state is positioned and further described as latch timing of the latch circuits 32A, 32B in cycles indicated with an asterisk (*) in the ~~column~~ row of the "completion signal" in Figs. 6, 8 and 10 to be described later.

Please amend page 28, 2nd paragraph as follows:

Fig. 5 illustrates an operational timing chart of a cache memory, which has the way prediction function but does not have the way selection determining function. Suppose here that five-time read accesses have been made from the CPU. Suppose further that although all the read data requested by the CPU exist on a way (W1), the history information is in such a state as to predict a way 0 (W0). In Fig. 5, the ~~column~~ row of the "CPU address" indicates effective addresses R1, R2, R3, R4 and R5 issued from the CPU, representing five kinds of access addresses. The ~~column~~ row of the "address array access" indicates for what address the access to the address array of the cache memory is made from the CPU. The ~~column~~ row of the "data access" indicates for what address the access to the data array of the cache memory is made from the CPU. The row of the "history information of predict[[ion]]ed way" describes what way predicted by the way prediction signal (22) based on what the hit-way history information instructs to select, where the way 0 and the way 1 is abbreviated as W0 and W1, respectively. The ~~column~~ row of the "way selected" describes what way the cache control part instructs to select in an actual situation via associative operation. The ~~column~~ row of the "location of the CPU requesting data" indicates the location of each access data requested by the CPU. The ~~column~~ row of the "CPU receiving data" indicates what way the data selected by the way selector and forwarded to the CPU belongs to. The data may be supplied from the external memory. The ~~column~~ row of the "access state" indicates whether each access from the CPU is a prediction miss, prediction hit or cache miss. The ~~column~~ row of the "external memory access" indicates in what cycle the external memory access is performed in the case of the cache miss. In the example of Fig. 5, the 5-time read accesses are all assumed as the prediction miss. As shown, R1

is found to be the prediction miss at time 1, and the access of R1 is completed at time 3. Then, R2 is found to be the prediction miss at time 4, and the access of R2 is completed at time 6. The following processing is performed in the same manner. In the case of Fig. 5, even when consecutive way prediction misses occur, the read access processing is completed every three cycles.